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Kind regards,

Team Nexperia
1. General description

The 74ALVT162823 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data or address paths of buses carrying parity.

The 74ALVT162823 has two 9-bit wide buffered registers with clock enable (\(n_{CE}\)) and master reset (\(n_{MR}\)) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding Q output of the flip-flop.

The 74ALVT162823 is designed with 30 Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers or transmitters.

2. Features

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- 5 V I/O compatible
- Ideal where high speed, light loading or increased fan-in are required with MOS microprocessors
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- Power-up reset
- Output capability: +12 mA to −12 mA
- Outputs include series resistance of 30 Ω making external termination resistors unnecessary
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883, method 3015: exceeds 2000 V
  - Machine Model: exceeds 200 V
3. Quick reference data

Table 1: Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH</td>
<td>propagation delay nCP to nQx</td>
<td>C_L = 50 pF; V_CC = 2.5 V</td>
<td>-</td>
<td>3.7</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_L = 50 pF; V_CC = 3.3 V</td>
<td>-</td>
<td>2.9</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>tPHL</td>
<td>propagation delay nCP to nQx</td>
<td>C_L = 50 pF; V_CC = 2.5 V</td>
<td>-</td>
<td>2.8</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_L = 50 pF; V_CC = 3.3 V</td>
<td>-</td>
<td>2.3</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>C_i</td>
<td>input capacitance</td>
<td>V_I = 0 V or V_CC</td>
<td>-</td>
<td>3</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>C_o</td>
<td>output capacitance</td>
<td>V_{IO} = 0 V or 3.0 V</td>
<td>-</td>
<td>9</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>I_{CC}</td>
<td>quiescent supply current</td>
<td>outputs disabled; V_CC = 2.5 V</td>
<td>-</td>
<td>40</td>
<td>-</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>outputs disabled; V_CC = 3.3 V</td>
<td>-</td>
<td>70</td>
<td>-</td>
<td>μA</td>
</tr>
</tbody>
</table>

4. Ordering information

Table 2: Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Temperature range</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>74ALVT162823DL</td>
<td>SSOP56</td>
<td>−40 °C to +85 °C</td>
<td>plastic shrink small outline package; 56 leads; body width 7.5 mm</td>
<td>SOT371-1</td>
<td></td>
</tr>
<tr>
<td>74ALVT162823DGG</td>
<td>TSSOP56</td>
<td>−40 °C to +85 °C</td>
<td>plastic thin shrink small outline package; 56 leads; body width 6.1 mm</td>
<td>SOT364-1</td>
<td></td>
</tr>
</tbody>
</table>
5. Functional diagram

![IEC logic symbol](image1)

**Fig 1. IEC logic symbol**

![Schematic of each output](image2)

**Fig 2. Schematic of each output**

![Bus hold circuit](image3)

**Fig 3. Bus hold circuit**
18-bit bus-interface D-type flip-flop with reset and enable; 3-state

Fig 4. Logic diagram
6. Pinning information

6.1 Pinning

![Fig 5. Pin configuration]

6.2 Pin description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1MR</td>
<td>1</td>
<td>master reset input (active LOW)</td>
</tr>
<tr>
<td>1OE</td>
<td>2</td>
<td>output enable input (active LOW)</td>
</tr>
<tr>
<td>1Q0</td>
<td>3</td>
<td>data output 0</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>1Q1</td>
<td>5</td>
<td>data output 1</td>
</tr>
<tr>
<td>1Q2</td>
<td>6</td>
<td>data output 2</td>
</tr>
<tr>
<td>VCC</td>
<td>7</td>
<td>supply voltage</td>
</tr>
<tr>
<td>1Q3</td>
<td>8</td>
<td>data output 3</td>
</tr>
</tbody>
</table>
Table 3: Pin description ...continued

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Q4</td>
<td>9</td>
<td>1 data output 4</td>
</tr>
<tr>
<td>1Q5</td>
<td>10</td>
<td>1 data output 5</td>
</tr>
<tr>
<td>GND</td>
<td>11</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>1Q6</td>
<td>12</td>
<td>1 data output 6</td>
</tr>
<tr>
<td>1Q7</td>
<td>13</td>
<td>1 data output 7</td>
</tr>
<tr>
<td>1Q8</td>
<td>14</td>
<td>1 data output 8</td>
</tr>
<tr>
<td>2Q0</td>
<td>15</td>
<td>2 data output 0</td>
</tr>
<tr>
<td>2Q1</td>
<td>16</td>
<td>2 data output 1</td>
</tr>
<tr>
<td>2Q2</td>
<td>17</td>
<td>2 data output 2</td>
</tr>
<tr>
<td>GND</td>
<td>18</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>2Q3</td>
<td>19</td>
<td>2 data output 3</td>
</tr>
<tr>
<td>2Q4</td>
<td>20</td>
<td>2 data output 4</td>
</tr>
<tr>
<td>2Q5</td>
<td>21</td>
<td>2 data output 5</td>
</tr>
<tr>
<td>VCC</td>
<td>22</td>
<td>supply voltage</td>
</tr>
<tr>
<td>2Q6</td>
<td>23</td>
<td>2 data output 6</td>
</tr>
<tr>
<td>2Q7</td>
<td>24</td>
<td>2 data output 7</td>
</tr>
<tr>
<td>GND</td>
<td>25</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>2Q8</td>
<td>26</td>
<td>2 data output 8</td>
</tr>
<tr>
<td>2OE</td>
<td>27</td>
<td>2 output enable input (active LOW)</td>
</tr>
<tr>
<td>2MR</td>
<td>28</td>
<td>2 master reset input (active LOW)</td>
</tr>
<tr>
<td>2CP</td>
<td>29</td>
<td>2 clock pulse input (active rising edge)</td>
</tr>
<tr>
<td>2CE</td>
<td>30</td>
<td>2 clock enable input (active LOW)</td>
</tr>
<tr>
<td>2D8</td>
<td>31</td>
<td>2 data input 8</td>
</tr>
<tr>
<td>GND</td>
<td>32</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>2D7</td>
<td>33</td>
<td>2 data input 7</td>
</tr>
<tr>
<td>2D6</td>
<td>34</td>
<td>2 data input 6</td>
</tr>
<tr>
<td>VCC</td>
<td>35</td>
<td>supply voltage</td>
</tr>
<tr>
<td>2D5</td>
<td>36</td>
<td>2 data input 5</td>
</tr>
<tr>
<td>2D4</td>
<td>37</td>
<td>2 data input 4</td>
</tr>
<tr>
<td>2D3</td>
<td>38</td>
<td>2 data input 3</td>
</tr>
<tr>
<td>GND</td>
<td>39</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>2D2</td>
<td>40</td>
<td>2 data input 2</td>
</tr>
<tr>
<td>2D1</td>
<td>41</td>
<td>2 data input 1</td>
</tr>
<tr>
<td>2D0</td>
<td>42</td>
<td>2 data input 0</td>
</tr>
<tr>
<td>1D8</td>
<td>43</td>
<td>1 data input 8</td>
</tr>
<tr>
<td>1D7</td>
<td>44</td>
<td>1 data input 7</td>
</tr>
<tr>
<td>1D6</td>
<td>45</td>
<td>1 data input 6</td>
</tr>
<tr>
<td>GND</td>
<td>46</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>1D5</td>
<td>47</td>
<td>1 data input 5</td>
</tr>
<tr>
<td>1D4</td>
<td>48</td>
<td>1 data input 4</td>
</tr>
<tr>
<td>1D3</td>
<td>49</td>
<td>1 data input 3</td>
</tr>
</tbody>
</table>
74AL VT162823
18-bit bus-interface D-type flip-flop with reset and enable; 3-state

7. Functional description

7.1 Function table

<table>
<thead>
<tr>
<th>Table 4: Function table [1]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating mode</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Clear</td>
</tr>
<tr>
<td>Load and read data</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Hold</td>
</tr>
<tr>
<td>High-impedance</td>
</tr>
</tbody>
</table>

[1] H = HIGH voltage level;
    h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
    L = LOW voltage level;
    l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
    NC = no change;
    X = don’t care;
    Z = high-impedance OFF-state;
    ↑ = LOW-to-HIGH clock transition;

8. Limiting values

<table>
<thead>
<tr>
<th>Table 5: Limiting values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>VCC</td>
</tr>
<tr>
<td>Vl</td>
</tr>
<tr>
<td>VO</td>
</tr>
<tr>
<td>IK</td>
</tr>
<tr>
<td>OK</td>
</tr>
</tbody>
</table>
9. Recommended operating conditions

Table 5: Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_O</td>
<td>output current</td>
<td>output in LOW-state</td>
<td>-128</td>
<td>-64</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>output in HIGH-state</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_stg</td>
<td>storage temperature</td>
<td></td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>T_J</td>
<td>junction temperature</td>
<td></td>
<td>[2]</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

Table 6: Recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_CC</td>
<td>supply voltage</td>
<td>V_CC supply voltage</td>
<td>2.3</td>
<td>-</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>V_I</td>
<td>input voltage</td>
<td>V_I input voltage</td>
<td>0</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>V_H</td>
<td>HIGH-level input voltage</td>
<td>V_H HIGH-level input voltage</td>
<td>1.7</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>V_L</td>
<td>LOW-level input voltage</td>
<td>V_L LOW-level input voltage</td>
<td>0.7</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>I_OH</td>
<td>HIGH-level output current</td>
<td>I_OH HIGH-level output current</td>
<td>-8</td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>I_OL</td>
<td>LOW-level output current</td>
<td>I_OL LOW-level output current</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>Δt/ΔV</td>
<td>input transition rise or fall rate</td>
<td>Δt/ΔV input transition rise or fall rate</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>ns/V</td>
</tr>
<tr>
<td>T_amb</td>
<td>ambient temperature</td>
<td>T_amb ambient temperature in free air</td>
<td>-40</td>
<td>-</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

V_CC = 3.3 V

| V_CC   | supply voltage       | V_CC supply voltage | 3.0  | -    | 3.6  | V    |
| V_I    | input voltage        | V_I input voltage  | 0    | -    | 5.5  | V    |
| V_H    | HIGH-level input voltage | V_H HIGH-level input voltage | 2.0  | -    | -    | V    |
| V_L    | LOW-level input voltage | V_L LOW-level input voltage | 0.8  | -    | -    | V    |
| I_OH   | HIGH-level output current | I_OH HIGH-level output current | -12  | -    | -    | mA   |
| I_OL   | LOW-level output current | I_OL LOW-level output current | 12   | -    | -    | mA   |
| Δt/ΔV  | input transition rise or fall rate | Δt/ΔV input transition rise or fall rate | 10   | -    | -    | ns/V |
| T_amb  | ambient temperature  | T_amb ambient temperature in free air | -40  | -    | +85  | °C   |
## 10. Static characteristics

### Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{CC}} = 2.5\ V \pm 0.2\ V$ [1]</td>
<td>$V_{\text{IK}}$ input diode voltage</td>
<td>$V_{\text{CC}} = 2.3\ V;\ I_{\text{Ik}} = -18\ mA$</td>
<td>-</td>
<td>-0.85</td>
<td>-1.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{OH}}$ HIGH-level output voltage</td>
<td>$V_{\text{CC}} = 2.3\ V;\ I_{\text{OH}} = -8\ mA$</td>
<td>1.7</td>
<td>2.5</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{OL}}$ LOW-level output voltage</td>
<td>$V_{\text{CC}} = 2.3\ V;\ I_{\text{OL}} = 12\ mA$</td>
<td>-</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{RST}}$ power-up LOW-state output voltage</td>
<td>$V_{\text{CC}} = 2.7\ V;\ I_{\text{Q}} = 1\ mA;\ V_{\text{I}} = V_{\text{CC}}$ or GND</td>
<td>[2]</td>
<td>0.2</td>
<td>0.55</td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{LI}}$</td>
<td>input leakage current</td>
<td>control pins $V_{\text{CC}} = 2.7\ V;\ V_{\text{I}} = \text{GND}$</td>
<td>-</td>
<td>0.1</td>
<td>±1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{CC}} = 2.7\ V;\ V_{\text{I}} = 5.5\ V$</td>
<td>-</td>
<td>0.1</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>data pins $V_{\text{CC}} = 2.7\ V;\ V_{\text{I}} = 5.5\ V$</td>
<td>[3]</td>
<td>0.1</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{CC}} = 2.7\ V;\ V_{\text{I}} = V_{\text{CC}}$</td>
<td>[3]</td>
<td>0.5</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{CC}} = 2.7\ V;\ V_{\text{I}} = 0\ V$</td>
<td>[3]</td>
<td>0.1</td>
<td>±5</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{OFF}}$</td>
<td>power-down output current</td>
<td>$V_{\text{CC}} = 0\ V;\ V_{\text{I}}$ or $V_{\text{O}} = 0\ V$ to 4.5 $V$</td>
<td>-</td>
<td>+0.1</td>
<td>±100</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{HOLD}}$</td>
<td>bus hold current data inputs</td>
<td>$V_{\text{CC}} = 2.5\ V;\ V_{\text{I}} = 0.7\ V$</td>
<td>[4]</td>
<td>10</td>
<td>-</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{CC}} = 2.5\ V;\ V_{\text{I}} = 1.7\ V$</td>
<td>[4]</td>
<td>-70</td>
<td>-</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{EX}}$</td>
<td>external current into output</td>
<td>output HIGH-state when $V_{\text{O}} &gt; V_{\text{CC}}$; $V_{\text{O}} = 5.5\ V;\ V_{\text{CC}} = 2.5\ V$</td>
<td>-</td>
<td>10</td>
<td>125</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{PU}}$</td>
<td>power-up 3-state output current</td>
<td>$V_{\text{CC}} \leq 1.2\ V;\ V_{\text{O}} = 0.5\ V$ to $V_{\text{CC}}$; $V_{\text{I}} = \text{GND}$ or $V_{\text{CC}}$</td>
<td>[5]</td>
<td>1</td>
<td>±100</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{PD}}$</td>
<td>power-down 3-state output current</td>
<td>$V_{\text{CC}} \leq 1.2\ V;\ V_{\text{O}} = 0.5\ V$ to $V_{\text{CC}}$; $V_{\text{I}} = \text{GND}$ or $V_{\text{CC}}$</td>
<td>[5]</td>
<td>1</td>
<td>±100</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{OZ}}$</td>
<td>3-state output current</td>
<td>$V_{\text{CC}} = 2.7\ V;\ V_{\text{I}} = V_{\text{IL}}$ or $V_{\text{IH}}$</td>
<td>-</td>
<td>0.5</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>output HIGH-state; $V_{\text{O}} = 2.3\ V$</td>
<td>-</td>
<td>0.5</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>output LOW-state; $V_{\text{O}} = 0.5\ V$</td>
<td>-</td>
<td>+0.5</td>
<td>-5</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{CC}}$</td>
<td>quiescent supply current</td>
<td>$V_{\text{CC}} = 2.7\ V;\ V_{\text{I}} = \text{GND}$ or $V_{\text{CC}}$; $I_{\text{O}} = 0\ A$</td>
<td>outputs HIGH-state</td>
<td>-</td>
<td>0.04</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>outputs LOW-state</td>
<td>-</td>
<td>2.7</td>
<td>4.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>outputs disabled</td>
<td>[6]</td>
<td>0.04</td>
<td>0.1</td>
<td>mA</td>
</tr>
<tr>
<td>$\Delta I_{\text{CC}}$</td>
<td>additional quiescent supply current per input pin</td>
<td>$V_{\text{CC}} = 2.3\ V$ to 2.7 $V$; one input at $V_{\text{CC}} = -0.6\ V$, other inputs at $V_{\text{CC}}$ or GND</td>
<td>[7]</td>
<td>0.04</td>
<td>0.4</td>
<td>mA</td>
</tr>
<tr>
<td>$C_{\text{i}}$</td>
<td>input capacitance</td>
<td>$V_{\text{I}} = 0\ V$ or $V_{\text{CC}}$</td>
<td>-</td>
<td>3</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{\text{o}}$</td>
<td>output capacitance</td>
<td>$V_{\text{IO}} = 0\ V$ or 3.0 $V$</td>
<td>-</td>
<td>9</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>$V_{\text{CC}} = 3.3\ V \pm 0.3\ V$ [8]</td>
<td>$V_{\text{IK}}$ input diode voltage</td>
<td>$V_{\text{CC}} = 3.0\ V;\ I_{\text{IK}} = -18\ mA$</td>
<td>-</td>
<td>0.85</td>
<td>−1.2</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{OH}}$</td>
<td>HIGH-level output voltage</td>
<td>$V_{\text{CC}} = 3.0\ V;\ I_{\text{OH}} = -12\ mA$</td>
<td>[8]</td>
<td>2.0</td>
<td>2.3</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{OL}}$</td>
<td>LOW-level output voltage</td>
<td>$V_{\text{CC}} = 3.0\ V;\ I_{\text{OL}} = 12\ mA$</td>
<td>-</td>
<td>0.5</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{RST}}$</td>
<td>power-up LOW-state output voltage</td>
<td>$V_{\text{CC}} = 3.6\ V;\ I_{\text{O}} = 1\ mA;\ V_{\text{I}} = V_{\text{CC}}$ or GND</td>
<td>[3]</td>
<td>-</td>
<td>0.55</td>
<td>V</td>
</tr>
</tbody>
</table>
Table 7: Static characteristics ...continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T amb = −40 °C to +85 °C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I LI</td>
<td>input leakage current</td>
<td>control pins</td>
<td>V CC = 3.6 V; V I = V CC or GND</td>
<td>-</td>
<td>0.1</td>
<td>±1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V CC = 0 V or 3.6 V; V I = 5.5 V</td>
<td>-</td>
<td>0.1</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>data pins</td>
<td>V CC = 3.6 V; V I = 5.5 V</td>
<td>[3]</td>
<td>0.1</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V CC = 3.6 V; V I = V CC</td>
<td>[3]</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V CC = 3.6 V; V I = 0 V</td>
<td>[3]</td>
<td>+0.1</td>
<td>−5</td>
</tr>
<tr>
<td>I OFF</td>
<td>power-down output current</td>
<td>V CC = 0 V; V I or V O = 0 V to 4.5 V</td>
<td>-</td>
<td>0.1</td>
<td>±100</td>
<td>µA</td>
</tr>
<tr>
<td>I HOLD</td>
<td>bus hold current data inputs</td>
<td>V CC = 3 V; V I = 0.8 V</td>
<td>9</td>
<td>75</td>
<td>130</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V CC = 3 V; V I = 2.0 V</td>
<td>9</td>
<td>−75</td>
<td>−140</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V CC = 3.6 V; V I = 0 V to 3.6 V</td>
<td>9</td>
<td>±500</td>
<td>0</td>
<td>µA</td>
</tr>
<tr>
<td>I EX</td>
<td>external current into output</td>
<td>output HIGH-state when V O &gt; V CC; V O = 5.5 V; V CC = 3.0 V</td>
<td>-</td>
<td>10</td>
<td>125</td>
<td>µA</td>
</tr>
<tr>
<td>I PU</td>
<td>power-up 3-state output current</td>
<td>V CC ≤ 1.2 V; V O = 0.5 V to V CC; V I = GND or V CC</td>
<td>10</td>
<td>-</td>
<td>1</td>
<td>±100</td>
</tr>
<tr>
<td>I PD</td>
<td>power-down 3-state output current</td>
<td>V CC ≤ 1.2 V; V O = 0.5 V to V CC; V I = GND or V CC</td>
<td>10</td>
<td>-</td>
<td>1</td>
<td>±100</td>
</tr>
<tr>
<td>I OZ</td>
<td>3-state output current</td>
<td>V CC = 3.6 V; V I = V IL or V IH</td>
<td>-</td>
<td>0.5</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>output HIGH-state; V O = 3.0 V</td>
<td>-</td>
<td>+0.5</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td>I CC</td>
<td>quiescent supply current</td>
<td>V CC = 3.6 V; V I = GND or V CC; I O = 0 A</td>
<td>-</td>
<td>0.05</td>
<td>0.1</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>outputs HIGH-state</td>
<td>-</td>
<td>0.05</td>
<td>0.1</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>outputs LOW-state</td>
<td>-</td>
<td>3.9</td>
<td>5.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>outputs disabled</td>
<td>9</td>
<td>0.06</td>
<td>0.1</td>
<td>mA</td>
</tr>
<tr>
<td>ΔI CC</td>
<td>additional quiescent supply current per input pin</td>
<td>V CC = 3 V to 3.6 V; one input at V CC − 0.6 V, other inputs at V CC or GND</td>
<td>7</td>
<td>0.04</td>
<td>0.4</td>
<td>mA</td>
</tr>
<tr>
<td>C i</td>
<td>input capacitance</td>
<td>V I = 0 V or V CC</td>
<td>-</td>
<td>3</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>C o</td>
<td>output capacitance</td>
<td>V IO = 0 V or 3.0 V</td>
<td>-</td>
<td>9</td>
<td>-</td>
<td>pF</td>
</tr>
</tbody>
</table>

[1] All typical values are at V CC = 2.5 V and T amb = 25 °C.
[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
[3] Unused pins at V CC or GND.
[5] This parameter is valid for any V CC between 0 V and 1.2 V with a transition time of up to 10 ms. From V CC = 1.2 V to V CC = 2.5 V ± 0.2 V a transition time of 100 µs is permitted. This parameter is valid for T amb = 25 °C only.
[6] I CC is measured with outputs pulled up to V CC or pulled down to ground.
[7] This is the increase in supply current for each input at the specified voltage level other than V CC or GND.
[8] All typical values are at V CC = 3.3 V and T amb = 25 °C.
[9] This is the bus hold overdrive current required to force the input to the opposite logic state.
[10] This parameter is valid for any V CC between 0 V and 1.2 V with a transition time of up to 10 ms. From V CC = 1.2 V to V CC = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T amb = 25 °C only.
## 11. Dynamic characteristics

### Table 8: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11; 
$T_{\text{amb}} = -40^\circ \text{C} \text{ to } +85^\circ \text{C}.$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{CC}} = 2.5 \text{ V} \pm 0.2 \text{ V}$ [1]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{PLH}}$</td>
<td>propagation delay nCP to nQx</td>
<td>see Figure 6</td>
<td>2.1</td>
<td>3.7</td>
<td>5.8</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PHL}}$</td>
<td>propagation delay nCP to nQx</td>
<td>see Figure 6</td>
<td>2.0</td>
<td>2.8</td>
<td>4.6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PHL}}$</td>
<td>propagation delay nMR to nQx</td>
<td>see Figure 8</td>
<td>2.0</td>
<td>3.0</td>
<td>4.6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>output enable time to HIGH-level nCP to nQx</td>
<td>see Figure 9</td>
<td>2.8</td>
<td>4.4</td>
<td>6.6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>output enable time to LOW-level nCP to nQx</td>
<td>see Figure 8</td>
<td>2.0</td>
<td>3.4</td>
<td>5.2</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>output enable time to LOW-level nCP to nQx</td>
<td>see Figure 10</td>
<td>2.3</td>
<td>3.2</td>
<td>4.6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>output enable time from HIGH-level see Figure 9</td>
<td>2.0</td>
<td>2.5</td>
<td>3.5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{su(H)}}$</td>
<td>set-up time HIGH nDx to nCP</td>
<td>see Figure 7</td>
<td>1.0</td>
<td>0.5</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{su(H)}}$</td>
<td>set-up time LOW nDx to nCP</td>
<td>see Figure 7</td>
<td>2.0</td>
<td>1.3</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{su(L)}}$</td>
<td>set-up time HIGH nCE to nCP</td>
<td>see Figure 7</td>
<td>1.0</td>
<td>0.2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{su(L)}}$</td>
<td>set-up time LOW nCE to nCP</td>
<td>see Figure 7</td>
<td>2.0</td>
<td>1.3</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{h(H)}}$</td>
<td>hold time HIGH nDx to nCP</td>
<td>see Figure 7</td>
<td>+0.1</td>
<td>-1.4</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{h(L)}}$</td>
<td>hold time LOW nDx to nCP</td>
<td>see Figure 7</td>
<td>+0.1</td>
<td>-0.5</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{h(L)}}$</td>
<td>hold time LOW nCE to nCP</td>
<td>see Figure 7</td>
<td>+1.0</td>
<td>-0.1</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{WH}}$</td>
<td>pulse width HIGH nCP</td>
<td>see Figure 6</td>
<td>2.0</td>
<td>0.8</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{WL}}$</td>
<td>pulse width LOW nCP</td>
<td>see Figure 6</td>
<td>3.0</td>
<td>2.1</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{WL}}$</td>
<td>pulse width LOW nMR</td>
<td>see Figure 8</td>
<td>2.0</td>
<td>0.8</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{rec}}$</td>
<td>recovery time nMR to nCP</td>
<td>see Figure 8</td>
<td>2.3</td>
<td>1.3</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

### $V_{\text{CC}} = 3.3 \text{ V} \pm 0.3 \text{ V}$ [2]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{PLH}}$</td>
<td>propagation delay nCP to nQx</td>
<td>see Figure 6</td>
<td>1.8</td>
<td>2.9</td>
<td>4.4</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PHL}}$</td>
<td>propagation delay nCP to nQx</td>
<td>see Figure 6</td>
<td>1.6</td>
<td>2.3</td>
<td>3.6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PHL}}$</td>
<td>propagation delay nMR to nQx</td>
<td>see Figure 8</td>
<td>1.8</td>
<td>2.5</td>
<td>3.7</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>output enable time to HIGH-level nCP to nQx</td>
<td>see Figure 9</td>
<td>2.0</td>
<td>3.5</td>
<td>5.2</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>output enable time to LOW-level nCP to nQx</td>
<td>see Figure 10</td>
<td>1.7</td>
<td>2.8</td>
<td>3.8</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>output enable time to LOW-level nCP to nQx</td>
<td>see Figure 9</td>
<td>2.4</td>
<td>3.5</td>
<td>4.7</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{PZH}}$</td>
<td>output enable time from LOW-level see Figure 10</td>
<td>1.9</td>
<td>2.8</td>
<td>3.8</td>
<td>ns</td>
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</table>
12. Waveforms

Table 8: Dynamic characteristics ...continued
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>( t_{SU(H)} )</td>
<td>set-up time HIGH</td>
<td>nDX to nCP</td>
<td>see Figure 7</td>
<td>1.0</td>
<td>0.5</td>
<td>- ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>nCE to nCP</td>
<td>see Figure 7</td>
<td>1.0</td>
<td>0.1</td>
<td>- ns</td>
</tr>
<tr>
<td>( t_{SU(L)} )</td>
<td>set-up time LOW</td>
<td>nDX to nCP</td>
<td>see Figure 7</td>
<td>1.6</td>
<td>1.1</td>
<td>- ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>nCE to nCP</td>
<td>see Figure 7</td>
<td>+0.5</td>
<td>-0.5</td>
<td>- ns</td>
</tr>
<tr>
<td>( t_{H(H)} )</td>
<td>hold time HIGH</td>
<td>nDX to nCP</td>
<td>see Figure 7</td>
<td>+0.1</td>
<td>-0.5</td>
<td>- ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>nCE to nCP</td>
<td>see Figure 7</td>
<td>1.0</td>
<td>-0.1</td>
<td>- ns</td>
</tr>
<tr>
<td>( t_{H(L)} )</td>
<td>hold time LOW</td>
<td>nDX to nCP</td>
<td>see Figure 7</td>
<td>+0.1</td>
<td>-0.7</td>
<td>- ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>nCE to nCP</td>
<td>see Figure 7</td>
<td>1.0</td>
<td>0.5</td>
<td>- ns</td>
</tr>
<tr>
<td>( t_{WH} )</td>
<td>pulse width HIGH nCP</td>
<td>see Figure 6</td>
<td>1.5</td>
<td>0.7</td>
<td>- ns</td>
<td></td>
</tr>
<tr>
<td>( t_{WL} )</td>
<td>pulse width LOW</td>
<td>nCP</td>
<td>see Figure 6</td>
<td>2.5</td>
<td>1.4</td>
<td>- ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>nMR</td>
<td>see Figure 8</td>
<td>2.0</td>
<td>1.5</td>
<td>- ns</td>
</tr>
<tr>
<td>( t_{REC} )</td>
<td>recovery time nMR to nCP</td>
<td>see Figure 8</td>
<td>2.0</td>
<td>1.1</td>
<td>- ns</td>
<td></td>
</tr>
</tbody>
</table>

[1] All typical values are measured at \( V_{CC} = 2.5 \) V and \( T_{amb} = 25 \) °C.
[2] All typical values are measured at \( V_{CC} = 3.3 \) V and \( T_{amb} = 25 \) °C.

Measurement points are given in Table 9.

\( V_{OH} \) is a typical voltage output drop that occur with the output load.

Fig 6. Propagation delay clock input (nCP) to output (nQx), clock pulse width and maximum clock frequency (nCP)
Measurement points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Data set-up and hold times

Measurement points are given in Table 9.

$V_{OH}$ is a typical voltage output drop that occur with the output load.

Fig 8. Master reset (MR) pulse width, propagation delay master reset (MR) to output (nQx) and master reset (MR) to clock (nCP) recovery time

Measurement points are given in Table 9.

$V_{OH}$ is a typical voltage output drop that occur with the output load.

Fig 9. 3-state output enable time to HIGH-level and output disable time from HIGH-level
Measurement points are given in Table 9.

$V_{OL}$ is a typical voltage output drop that occur with the output load.

Fig 10. 3-state output enable time to LOW-level and output disable time from LOW-level

Table 9: Measurement points

<table>
<thead>
<tr>
<th>Supply voltage</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_M$</td>
<td>$V_M$</td>
</tr>
<tr>
<td>$\geq 3 \text{ V}$</td>
<td>1.5 V</td>
<td>$V_{OL} + 0.3 \text{ V}$</td>
</tr>
<tr>
<td>$\leq 2.7 \text{ V}$</td>
<td>$0.5 \times V_{CC}$</td>
<td>$V_{OL} + 0.3 \text{ V}$</td>
</tr>
</tbody>
</table>
Measurement points are given in Table 9.

a. Input pulse definition

Test data is given in Table 10.

Definitions test circuit:

RL = Load resistor.

CL = Load capacitance including jig and probe capacitance.

RT = Termination resistance should be equal to output impedance Zo of the pulse generator.

VEXT = Test voltage for switching times.

b. Test circuit

Fig 11. Load circuitry for switching times

Table 10: Test data

<table>
<thead>
<tr>
<th>Input</th>
<th>f1</th>
<th>tW</th>
<th>tr, tf</th>
<th>tPLZ, tPZL</th>
<th>tPLH, tPHL</th>
<th>tPHZ, tPZH</th>
<th>VEXT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>3.0 V or VCC whichever is less</td>
<td>≤ 10 MHz</td>
<td>500 ns</td>
<td>≤ 2.5 ns</td>
<td>6 V or 2 × VCC</td>
<td>open</td>
<td>GND</td>
</tr>
</tbody>
</table>
13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

DIMENSIONS (mm are the original dimensions)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A max.</th>
<th>A</th>
<th>A</th>
<th>A</th>
<th>b</th>
<th>c</th>
<th>D (1)</th>
<th>E (1)</th>
<th>e</th>
<th>H E</th>
<th>L</th>
<th>L P</th>
<th>Q</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>Z (1)</th>
<th>θ</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>2.8</td>
<td>0.4</td>
<td>0.2</td>
<td>0.25</td>
<td>0.3</td>
<td>0.22</td>
<td>18.55</td>
<td>18.30</td>
<td>0.635</td>
<td>10.4</td>
<td>1.4</td>
<td>1.0</td>
<td>1.2</td>
<td>0.25</td>
<td>0.18</td>
<td>0.1</td>
<td>0.85</td>
<td>0.40</td>
</tr>
<tr>
<td></td>
<td>0.2</td>
<td>2.20</td>
<td>0.25</td>
<td>0.2</td>
<td>0.13</td>
<td>7.6</td>
<td>7.4</td>
<td>10.1</td>
<td>1.0</td>
<td>0.635</td>
<td>10.4</td>
<td>1.4</td>
<td>1.0</td>
<td>1.2</td>
<td>0.25</td>
<td>0.18</td>
<td>0.1</td>
<td>0.85</td>
</tr>
<tr>
<td></td>
<td>0.2</td>
<td>2.35</td>
<td>0.25</td>
<td>0.2</td>
<td>0.13</td>
<td>18.55</td>
<td>18.30</td>
<td>0.635</td>
<td>10.4</td>
<td>1.4</td>
<td>1.0</td>
<td>1.2</td>
<td>0.25</td>
<td>0.18</td>
<td>0.1</td>
<td>0.85</td>
<td>0.40</td>
<td></td>
</tr>
</tbody>
</table>

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

Fig 12. Package outline SOT371-1 (SSOP56)
Philips Semiconductors

74ALVT162823

18-bit bus-interface D-type flip-flop with reset and enable; 3-state

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

DIMENSIONS (mm are the original dimensions).

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<th></th>
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<tbody>
<tr>
<td>mm</td>
<td>1.2</td>
<td>0.15</td>
<td>0.15</td>
<td>0.25</td>
<td>0.28</td>
<td>0.17</td>
<td>0.2</td>
<td>14.1</td>
<td>6.2</td>
<td>0.5</td>
<td>6.3</td>
<td>7.9</td>
<td>1</td>
<td>0.8</td>
<td>0.4</td>
<td>0.50</td>
<td>0.35</td>
<td>0.25</td>
</tr>
</tbody>
</table>

Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION

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<th>REFERENCES</th>
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<tr>
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EUROPEAN PROJECTION

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Fig 13. Package outline SOT364-1 (TSSOP56)
14. Revision history

Table 11: Revision history

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<th>Data sheet status</th>
<th>Change notice</th>
<th>Doc. number</th>
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Modifications:
- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.
- Section 2 “Features”: modified ‘Jedec Std 17’ into ‘JESD78’
- Table 1 and Table 8: changed propagation delays.

<table>
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15. Data sheet status

<table>
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<th>Data sheet status</th>
<th>Product status</th>
<th>Definition</th>
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<tbody>
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<td>Objective data</td>
<td>Development</td>
<td>This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.</td>
</tr>
<tr>
<td>II</td>
<td>Preliminary data</td>
<td>Qualification</td>
<td>This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.</td>
</tr>
<tr>
<td>III</td>
<td>Product data</td>
<td>Production</td>
<td>This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued data sheet before initiating or completing a design.
[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com
## 20. Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 General description</td>
<td>1</td>
</tr>
<tr>
<td>2 Features</td>
<td>1</td>
</tr>
<tr>
<td>3 Quick reference data</td>
<td>2</td>
</tr>
<tr>
<td>4 Ordering information</td>
<td>2</td>
</tr>
<tr>
<td>5 Functional diagram</td>
<td>3</td>
</tr>
<tr>
<td>6 Pinning information</td>
<td>5</td>
</tr>
<tr>
<td>6.1 Pinning</td>
<td>5</td>
</tr>
<tr>
<td>6.2 Pin description</td>
<td>5</td>
</tr>
<tr>
<td>7 Functional description</td>
<td>7</td>
</tr>
<tr>
<td>7.1 Function table</td>
<td>7</td>
</tr>
<tr>
<td>8 Limiting values</td>
<td>7</td>
</tr>
<tr>
<td>9 Recommended operating conditions</td>
<td>8</td>
</tr>
<tr>
<td>10 Static characteristics</td>
<td>9</td>
</tr>
<tr>
<td>11 Dynamic characteristics</td>
<td>11</td>
</tr>
<tr>
<td>12 Waveforms</td>
<td>12</td>
</tr>
<tr>
<td>13 Package outline</td>
<td>16</td>
</tr>
<tr>
<td>14 Revision history</td>
<td>18</td>
</tr>
<tr>
<td>15 Data sheet status</td>
<td>19</td>
</tr>
<tr>
<td>16 Definitions</td>
<td>19</td>
</tr>
<tr>
<td>17 Disclaimers</td>
<td>19</td>
</tr>
<tr>
<td>18 Trademarks</td>
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</tr>
<tr>
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<td>19</td>
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</table>